CLAIMS

What is claimed is:

1. A method for outputting a datastream processed by a processing device, the datastream processed by the processing device being output at a certain output clock rate, comprising:

supplying the datastream processed by the processing device to a memory device;

monitoring the loading level of the memory device; and

adjusting, as a function of the loading level of the memory device, the output clock rate at which the data of the datastream are output from the memory device.

2. The method of Claim 1, further comprising:

writing the data of the datastream processed by the processing device into the memory device at a write clock rate which is greater than the maximum rate of the datastream supplied to the processing device.

3. The method of Claim 1, further comprising:

varying the output clock rate between a first output clock rate and a second output clock rate as a function of the loading level of the memory device, the first output clock rate being lower than the minimum clock rate of the datastream supplied to the processing device, and the second output clock rate being higher than the maximum clock rate of the datastream supplied to the processing device.

4. The method of Claim 3, wherein the first output clock rate is used as output clock rate if the loading level of the memory device is lower than a predetermined limit value, whereas the second output clock rate is used as output clock rate if the loading level of the memory device is higher than the limit value.

5. The method of Claim 3, wherein the output clock rate is continuously adapted as a function of the loading level of the memory device, the output clock rate being increased with increasing loading level of the memory device.

6. The method of Claim 1, wherein a memory stack is used as memory device.

7. An apparatus for outputting a datastream processed by a processing device, the data of the datastream being supplied to the processing device at a certain input clock rate and must be output at a certain output clock rate, comprising:

a memory device which is supplied with the datastream processed by the processing device; and

a control device for monitoring the loading level of the memory device in order to adjust, as a function of the loading level of the memory device, the output clock rate, at which the data of the datastream are to be output out of the memory device.

8. The apparatus of Claim 7, wherein the data of the datastream processed by the processing device are supplied to the memory device at a certain write clock rate which is higher than the maximum input clock rate of the data stream supplied to the processing device.

9. The apparatus of Claim 7, wherein the control device changes the output clock rate of the memory device between a first output clock rate and a second output clock rate as a function of the loading level of the memory device, the first output clock rate being lower than the minimum input clock rate of the datastream supplied to the processing device, whereas the second output clock rate is higher than the maximum input clock rate of the datastream supplied to the processing device.

10. The apparatus of Claim 9, further comprising:

a switching device driven by the control device, the control device driving the switching device as a function of the loading level of the memory device in such a manner that the memory device is supplied with the first output clock rate as output clock rate via the switching device if the loading level of the memory device is lower than a predetermined limit value, whereas the memory device is supplied with the second output clock rate as output clock rate if the loading level of the memory device is higher than the limit value.

11. The apparatus of Claim 9, further comprising:

a clock generating device which, responsive to the control device, adjusts the output clock rate of the memory device.

12. The apparatus of Claim 11, wherein the control device drives the clock generating device in such a manner that the output clock rate, generated by the clock generating device for the memory device, is increased with increased loading level of the memory device.

13. The apparatus of Claim 7, wherein the memory device is a memory stack.

14. The apparatus of Claim 1, wherein the memory device is a FIFO memory.

15. The apparatus of Claim 7, wherein the processing device is a decoding device.

16. The apparatus of Claim 15, wherein the processing device is an MPEG audio decoding device for decoding an MPEG audio datastream.